REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-20 are now in the application. Claims 1-20 are subject to examination and claims 21-25, which were previously withdrawn from examination, have been canceled. Claims 1, 2, 4, 5, 7, 10, and 12 have been amended. No new matter has been added.

It is noted that the Examiner, in the second paragraph on page 2 of the above-identified Office Action, did not state all of the claims currently pending in this application. The Examiner stated that "...claim 1...and claims 2-9 and 11-19...are currently pending in the application." However, applicants respectfully point out that claims 1-20 are currently pending in the instant application. Claims 10 and 20 were inadvertently omitted by the Examiner.

In the first paragraph under "Claim Rejections - 35 U.S.C. § 112" on page 2 of the above-identified Office Action, claims 1-20 have been rejected as being indefinite under 35 U.S.C. § 112, second paragraph.

More specifically, the Examiner again states that the use of the term "spacer layer" in claim 1 is inconsistent with the "usual meaning of that term." The Examiner states that the term is used "in claim 1 to mean 'separation/filler' while the accepted meaning (of "spacer layer") is 'sidewall spacer'." The Examiner has not shown any support for his statements regarding applicants' use of the term "spacer" and suggests using "separation" instead of "spacer", and further states that "a spacer layer is generally understood to mean a layer on the sidewalls of a gate and a separation layer is generally understood to mean a layer that separates two other elements." Nor has the Examiner cited any support for his belief as to the general understanding of the meaning of "spacer."

Moreover, the remarks attributed to applicants by the Examiner at the top of page 3 of the above-identified Office Action were not stated by applicants in the last response filed on June 6, 2003.

While applicants respectfully disagree with the Examiner's statements and submit that they are not using the term (spacer layer) inconsistently with its normal meaning, applicants have amended the claims to recite --separation-- instead of "spacer" as suggested by the Examiner, to facilitate prosecution. The wording "or separation" has been added two

locations in the specification to provide literal support for the new claim language.

It is accordingly believed that the claims meet the requirements of 35 U.S.C. § 112, second paragraph. The above remarks and claim changes are provided solely for the purpose of explaining the present invention. They are neither provided for overcoming the prior art nor do they narrow the scope of the claim for any reason related to the statutory requirements for a patent.

In the last full paragraph on page 3 of the Office action, claims 1-2 and 4-20 have been rejected as being unpatentable over Chang et al. (U.S. Pat. No. 6,365,465), presumably the Examiner intended to refer to Chan et al. because the '465 patent is in the name of Chan et al., (hereinafter "Chan") in view of Burghartz et al. (U.S. Patent No. 5,461,250) (hereinafter "Burghartz") under 35 U.S.C. § 103(a).

The rejection has been noted and the claims have been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found on page 14, lines 8-18 and page 15, lines 17-21, and in the original claims and drawings of the instant application.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, inter alia, a method for fabricating a

double gate MOSFET, which has the steps in the following sequence for producing gates aligned accurately with one another:

providing a substrate structure having a silicon substrate layer;

patterning the semiconductor layer resulting in a semiconductor layer structure provided as a channel of the double gate MOSFET;

depositing a second separation layer on the semiconductor layer structure and the first separation layer;

completely embedding the semiconductor layer structure in the first and second separation layers by patterning the first and second separation layers;

depositing a second insulation layer on a structure formed of the first and second separation layers;

vertically etching two depressions disposed along one direction, the two depressions dimensioned such that the semiconductor layer structure is situated completely between them, during the etching of the two depressions, the second insulation layer, the first and second separation layers and,

in each case on both sides, an edge section of the semiconductor layer structure being etched through completely in each case;

filling the depressions with an electrically conductive material;

forming a contact hole in the second insulation layer;

removing a region of the separation layers extending from the contact hole to the semiconductor layer structure and in which region the semiconductor layer structure is embedded in the separation layers by etching the region of the separation layers through the contact hole;

applying third insulation layers on inner walls of ~~a~~ the region of removed separation layers and on surfaces of the semiconductor layer structure; and

introducing a further electrically conductive material into the region of the removed separation layers.

Accordingly, the present invention is directed to a method for fabricating a double gate MOSFET transistor in a particular sequence. A semiconductor layer structure of a transistor channel is fully embedded in a spacer material, and is contact-connected by source and drain regions (which are filled into depressions that are etched on opposite sides of the semiconductor layer structure). Next, the spacer material is etched out selectively, and is replaced by the electrically conductive gate electrode material. The new and advantageous result of the method according to the present claimed invention is producing gate electrodes that are very accurately aligned with one another

Chan discloses a method for forming a double-gate MOSFET transistor. The method utilizes a selective lateral epitaxial growth of silicon from an existing single crystal silicon MOSFET channel to form the source/drain regions. The source/drain regions are bounded by pre-defined dielectric boundaries and are thereby limited in size to the local source/drain regions.

The dielectric which bounds the selective epitaxial growth is used as a self-aligned implant mask for selectively forming the heavily doped source/drain regions. The dielectric is removed after the source/drain formation to form a suspended silicon channel. The gate insulator and the gate electrodes are subsequently formed to complete the MOSFET.

There are clear differences between the fabrication method of the present claimed invention and that of Chan. The manner of forming the structure of Chan is totally different from the claimed method. In the present invention, the first and second spacer layers are patterned such that the semiconductor layer structure **remains completely embedded in the first and second spacer layers.** In contrast to Chan, the present invention discloses that the channel forming layer 4A is completely embedded by the layers 3 and 5. See Fig. 4 of the instant application. The Examiner acknowledges that Chan is deficient is this respect and attempts to make up for the deficiency with the disclosure of Burghartz. Additionally, claim 1 recites that the steps according to the present invention are **performed in the recited sequence,** which enables obtaining the advantages and benefits of the present invention, namely, an accurate alignment of the gates (topside and underside) in a technologically uncomplicated and relatively simple manner. This result is now recited in claim

1. Thus, for example, after the recited step of "patterning the semiconductor layer resulting in a semiconductor layer provided as a channel of the double gate MOSFET", the next step that follows is a step of "depositing a second separation layer on the semiconductor layer structure and the first separation layer." This is not true of Chan in which there is no depositing step of a second separation layer after the patterning step (shown in Fig. 2g of Chan), as recited in claim 1 of the instant application. Further, Chan does not show "removing a region of the separation layers extending from the contact hole to the semiconductor layer structure and in which region the semiconductor layer structure is embedded in the separation layers by etching the region of the separation layers through the contact hole" as recited in claim 1.

Burghartz discloses a dual gate thin film MOSFET device having multiple semiconductor layers sandwiched by semiconductor layers with different energy band structure to automatically confine carriers to the channel layers without the need for channel grading or modulation doping.

Burghartz does not overcome the deficiencies of Chan. Nor is Burghartz properly combinable with Chan.

While the Examiner has pointed to specific provisions of secondary Burghartz reference as allegedly providing basis for combining the references, the Examiner has not shown any reason in the primary Chan reference why one skilled in the art would even want to modify Chan in the first instance as suggested by the Examiner. It is inconceivable that one skilled in the art would identify the secondary Burghartz reference and then search the prior art and find the primary Chan reference and then modify it as proposed. It is respectfully submitted that the only reason for combining Chan and Burghartz is hindsight reconstruction of the prior art after having read applicants' disclosure.

It is submitted that the Examiner has not shown and articulated sufficient teaching, motivation, or suggestion in the prior art and particularly in the primary Chan reference for combining Chan and Burghartz as proposed.

Further, it is submitted that the claimed sequence of steps results in a new and advantageous result, namely the very accurate alignment of the gate electrodes which has not been heretofore achieved in the prior art. Therefore, the claimed sequence should be afforded patentable weight and not dismissed as the Examiner has done in the above-identified Office Action.

Clearly, the references do not show or teach "a method for fabricating a double gate MOSFET, which comprises the steps in the following sequence for producing gates aligned accurately with one another: providing a substrate structure having a silicon substrate layer; patterning the semiconductor layer

resulting in a semiconductor layer structure provided as a channel of the double gate MOSFET; depositing a second separation layer on the semiconductor layer structure and the first separation layer; completely embedding the semiconductor layer structure in the first and second separation layers by patterning the first and second separation layers; depositing a second insulation layer on a structure formed of the first and second separation layers; vertically etching two depressions disposed along one direction, the two depressions dimensioned such that the semiconductor layer structure is situated completely between them, during the etching of the two depressions, the second insulation layer, the first and second separation layers and, in each case on both sides, an edge section of the semiconductor layer structure being etched through completely in each case; filling the depressions with an electrically conductive material; forming a contact hole in the second insulation layer; removing a region of the separation layers extending from the contact hole to the semiconductor layer structure and in which region the

semiconductor layer structure is embedded in the s paration layers by etching the region of the separation layers through the contact hole;; applying third insulation layers on inner walls of a region of removed separation layers and on surfaces of the semiconductor layer structure; and introducing a further electrically conductive material into the region of the removed separation layers", as recited in claim 1 of the instant application.

In the second paragraph on page 8 of the Office Action, claim 3 has been rejected as being obvious over Chan in view of Shimizu (U.S. Pat. No. 5,753,541) under 35 U.S.C. § 103(a).

The foregoing discussion of Chan is equally applicable in the rejection of claim 3, which depends from claim 1.

Shimizu discloses a method for fabricating a thin film transistor with a high carrier mobility and a high on/off ration. Nor is Shimizu properly combinable with Chan.

While the Examiner has pointed to specific provisions of secondary Shimuzu reference as allegedly providing basis for combining the references, the Examiner has not shown any reason in the primary Chan reference why one skilled in the art would even want to modify Chan in the first instance as

suggested by the Examiner. It is inconceivable that one skilled in the art would identify the secondary Shimuzu reference and then search the prior art and find the primary Chan reference and then modify it as proposed. It is respectfully submitted that the only reason for combining Chan and Shimuzu is hindsight reconstruction of the prior art after having read applicants' disclosure.

Shimizu does not overcome the deficiencies of Chan (and Burghartz, even if the Examiner relied on the latter reference, which he has not, as an additional secondary reference in the rejection of claim 3).

Upon evaluation of the Examiner's comments, it is respectfully believed that the evidence adduced by the Examiner is insufficient to establish a prima facie case of obviousness with respect to the claims. Accordingly, the Examiner is requested to withdraw the rejection.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1.

In view of the foregoing, reconsideration and allowance of claims 1-20 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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For Applicants

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